32GB WT microSD Datasheet

PN:

TMMSDB032GV10TM-00N0

Revision History

Rev.	Date	Changes	Editor
1.0	2024/08/07	Document Create.	Yufeng Zhang
/	/	/	/

CONTENT

1 Overview

1.1 Product Description

The microSD communication is based on an advanced 9 and 8-pin interface (SD: 9pin, microSD: 8pin) designed to operate in at maximum operating frequency of 208MHz and 2.7V ~ 3.6V operating voltage range with 2 Type signaling (1.8V & 3.3V). More detail information on the interface, and mechanical description is defined as a part of this specification.

UHS-I and High Speed mode limited on this Specification.

The microSD Cards are fully compatible with Physical Layer Specification, support Ultra High Speed(UHS), provides high write/read speed and high IOPS, It was designed to meet the security, high capacity, high performance and environmental requirements inherent in next generation

consumer electronic devices.

The SD card system is a new mass-storage system based on innovations in semiconductor technology. It has been developed to provide an

inexpensive, mechanically robust storage medium in card form for multimedia consumer applications. SD card allows the design of inexpensive players and drivers without moving parts. A low power consumption and a wide supply voltage range favors consumer electronic devices.

- Ultra High Speed (UHS) Card
- It provides up to 104MB/s* performance. UHS cards are backward compatible on non-UHS hosts.
- Based on internal testing, performance may vary depending upon host device.
- 1 megabyte (MB) =1,000,000bytes.

1.2 Features Summary

- Complies to SD specifications version 3.0 or above
- Voltage operating: 2.7~3.6V.
- Targeted for portable and stationary applications
- Greater Performance Choices
- Bus Speed Mode:
  - DS-Default Speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5MB/sec
  - HS-High Speed mode: 3.3V signaling, frequency up to 50MHz, up to 25MB/sec
  - SDR12-1.8V signaling, frequency up to 25MHz, up to 12.5MB/sec
  - SDR25-1.8V signaling, frequency up to 50MHz, up to 25MB/sec
  - SDR50-1.8V signaling, frequency up to 100MHz, up to 50MB/sec
  - SDR104-1.8V signaling, frequency up to 208MHz, up to 104MB/sec
  - DDR50-1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50MB/s
- Switch function command supports Bus Speed Mode, Command System, Drive Strength, and future functions.
- Password protection (CMD42-LOCK_UNLOCK)
- Sophisticated system for error recovery including a powerful ECC
- Global Wear Leveling
- Power management for low power operation
- Add TF card adapter can be used in SD card socket

2 Pin Assignment

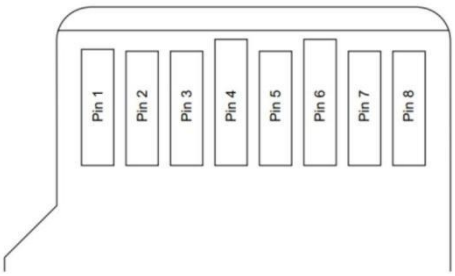

Table 1. Pin Assignment

Pin No.	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line [Bit 2]	RSV		Reserved
2	CD/DAT3	I/O/PP	Card Detect / Data Line [Bit 3]	CS	I	Chip Select
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit 1]	RSV		Reserved

Note:

S: power supply; I: input; O: output; PP: I/O using push -pull drivers

3 Product List

Table 2. Product List

Part Number	Capacity	Actual Size (Minimum)	Speed Class[1]	Write/Read Speed (Up to)[2]	UHS-I Mode	Type
TMMSDB032GV10TM-00N0	32GB	28.8GB	C10 U1 V10 A1	Up to 25/99 MB/s	SDR104	microSDHC

Note1:

● Measurement based on VTE3100 & VTE4100 TestMetrix device, SW 3.2A software or up version. The card must be reformatted between each script test.

● Test scripts:

- SD_Card (Spec3.0-4.0 HC & XC -UHS-I) SD 3.0 Speed Class (Grade 1/3) [rev32A].vte

- SD [Spec 5.1_HC&XC_UHS-I] Speed Class (Grade 1) & VSC_6_10_30 [VTE4100, Rail_UHS-I+II] SK1 [5.2.0.2-52B-A05].vte

- SD [Spec 5.1_HC&XC_UHS-I] A1/A2 Test - SDR50 (w CMD12_DB) [VTE4100, Rail_UHS-I+II] SK1 [5.2.0.1-52A-A00].vte Note2:

● Measurement based on VTE3100 & VTE4100 TestMetrix device, SW 3.2A software or up version. The card must be reformatted between eachscript test.

● Test scripts:

- SD_Card(Spec3.0_High&Extended-Capacity_UHS-I and Non-UHS-I)_Compliance [rev32A]-B87.vte

- SD_Card (Spec2.0-3.0 High&Extended-Capacity_UHS-I) Performance-Speed (Multiple Block Sequential) [rev31M] - SDR104-With Background Data.vte

● Maximum speed differs from the bus I/F speed. It varies depending upon the card performance. The average speed that a device writes to an SD

memory card may vary depending upon the device and the operation it is performing. Normal and high-speed cards can also be used with UHS-I host devices, but the high performance enabled by a UHS-I host device can only be achieved with a UHS-I memory card.

Note3:

● The products engineered with proprietary technology to reach speeds beyond UHS-I 104MB/s, require compatible devices capable of reaching such speeds. Based on internal testing, performance may be lower depending upon host device, interface, usage conditions, and other factors.

● Test Condition: Internal test

4 Current Consumption

Standby current: 600uA（Maximum value）

Standby current: 500uA（average value）

Operating current: 350mA（Maximum value）

Operating current: 300mA（average value）

*Test condition: Realtek5308 card reader (Voltage 3.3V), Fluke289C multi-meter.

5 Bus Operation Conditions

5.1 For 3.3V Signaling

5.1.1 Threshold Level for High Voltage Range

Table 3. Threshold Level for High Voltage

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75* V_{DD}		V	I_{OH}=2mA $V_{DD\ min}$
Output Low Voltage	V_{OL}		0.125* V_{DD}	V	I_{OL}=2mA $V_{DD\ min}$
Input High Voltage	V_{IH}	0.625* V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25* V_{DD}	V	
Power Up Time			250	ms	From 0V to $V_{DD\ min}$

5.1.2 Peak Voltage and Leakage Current

Table 4. Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

5.1.3 Bus Signal Line Load

Table 5. Bus Operating Conditions - Signal Line's Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	KΩ	To prevent bus floating
Total bus capacitance for each signal line	CL		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30pF
Card capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal inductance			16	nH	
Pull-up resistance inside card(pin1)	R_{DAT3}	10	90	KΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

5.1.4 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

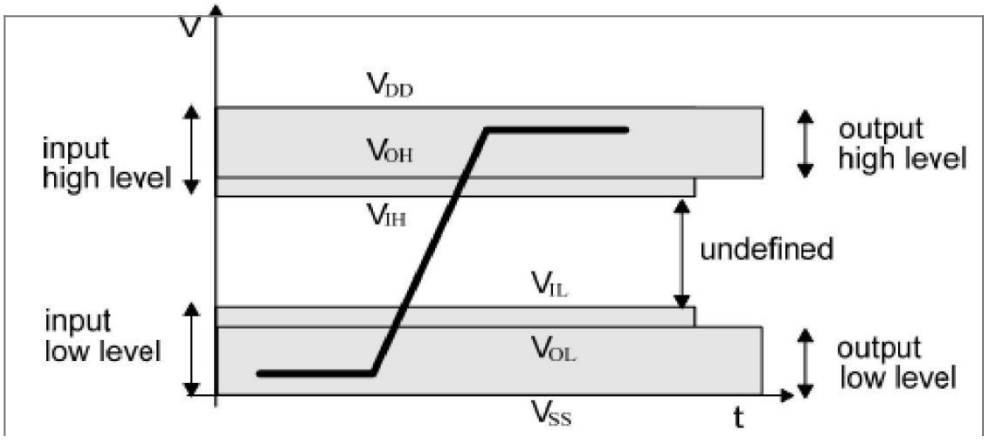

Figure 1. Bus Signal Levels

To meet the requirements of the JEDEC specification JESD8-1A and JESD8-7, the card input and output voltages shall be within the specified ranges shown in Table 6 for any V_{DD} of the allowed voltage range.

5.1.5 Bus Timing(Default)

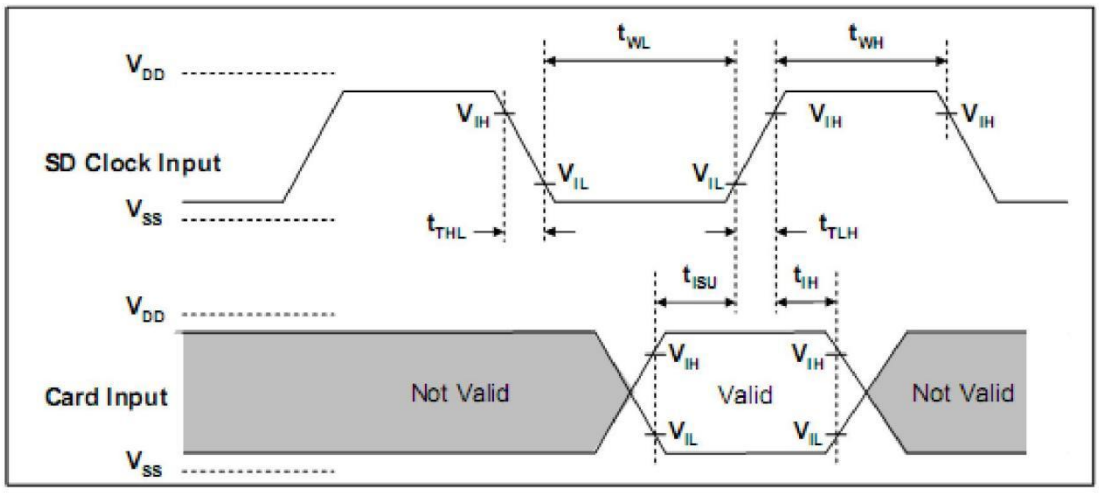

Figure 2. Card input Timing (Default Speed Card)

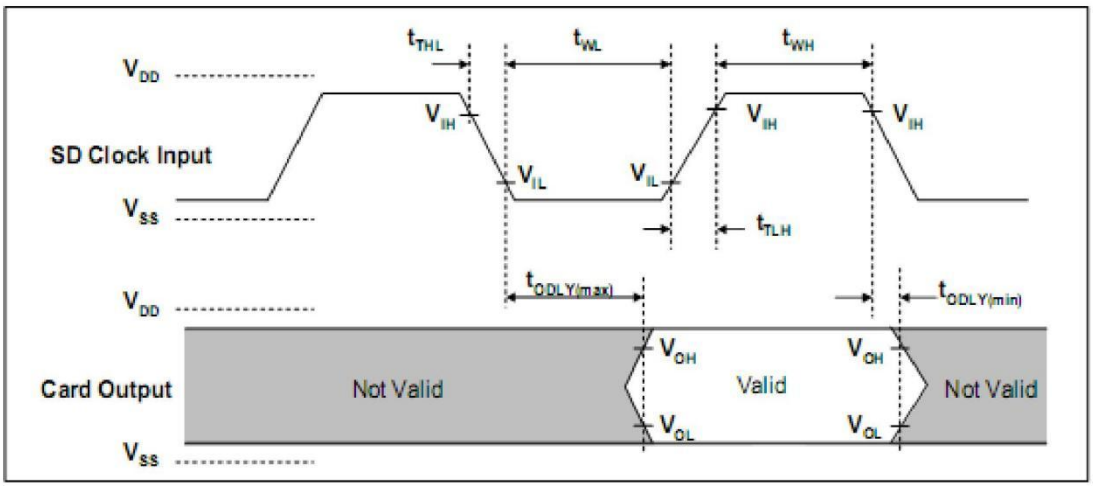

Figure 3. Card Output Timing (Default Speed Mode)

Table 6. Bus Timing-Parameters Values (Default Speed)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK （All values are referred to min（V_{IH}）and max（V_{IL}））					
Clock frequency Data Transfer Mode	fpp	0	25	MHz	C_{CARD} ≤ 10pF (1 card)
Clock frequency Identification Mode	f_{OD}	0[1]/100	400	KHz	C_{CARD} ≤ 10pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD} ≤ 10pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD} ≤ 10pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD} ≤ 10pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD} ≤ 10pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{CARD} ≤ 10pF (1 card)
Input hold time	t_{IH}	5		ns	C_{CARD} ≤ 10pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L ≤ 40pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L ≤ 40pF (1 card)

Note1:

0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required (refer to Chapter 4.4 -Clock Control in Physical Layer Specification)

5.1.6 Bus Timing (High-Speed Mode)

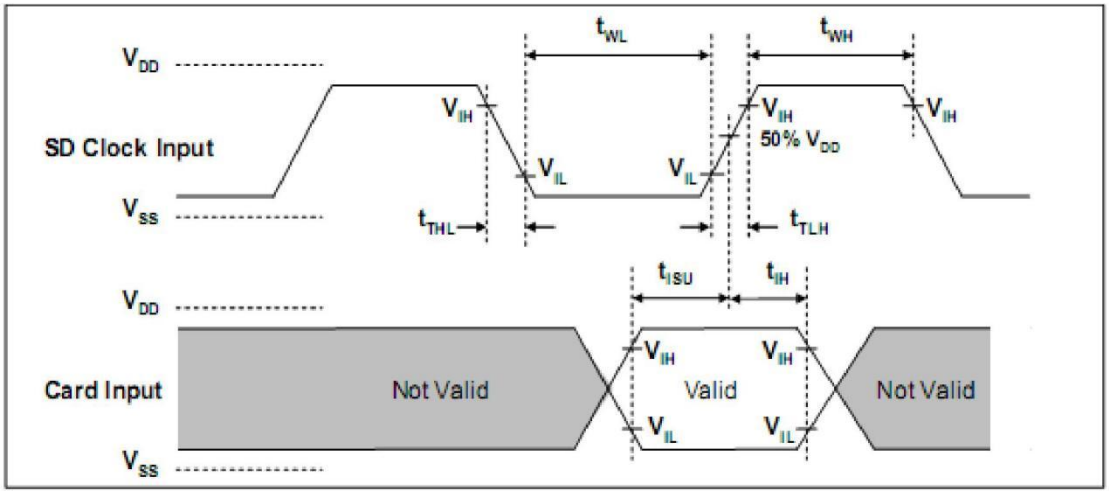

Figure 4. Card Input Timing(High Speed Card)

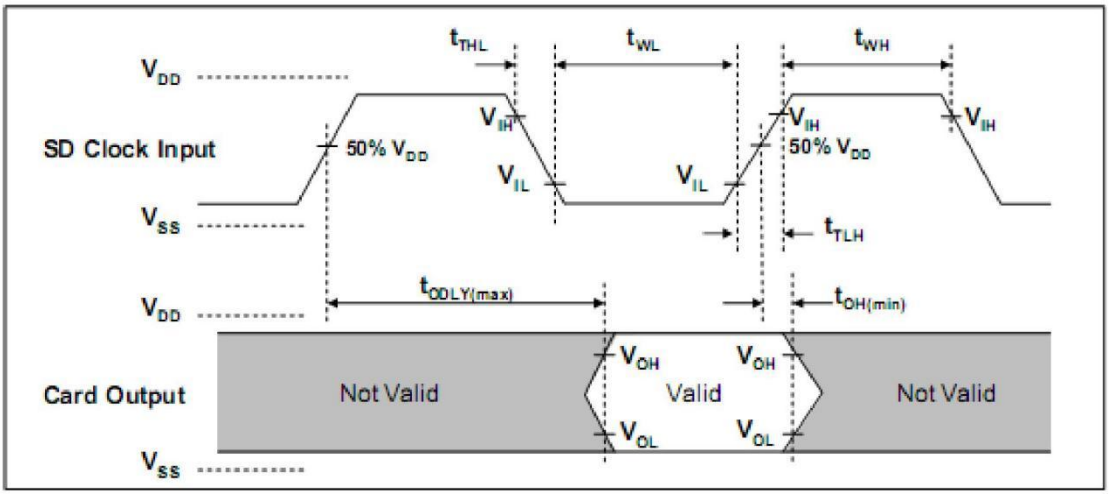

Figure 5. Card Output Timing(High Speed Mode)

Table 7. Bus Timing - Parameters Values (High Speed)

Parameter[1]	Symbol	Min.	Max	Unit	Remark
Clock CLK （All values are referred to min (V_{IH})and max (V_{IL}))					
Clock frequency data transfer Mode	fpp	0		MHz	C_{CARD} ≤ 10pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD} ≤ 10pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD} ≤ 10pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD} ≤ 10pF (1 card)
Clock fall time	t		3	ns	C_{CARD} ≤ 10pF (1 card)
CMD, (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD} ≤ 10pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD} ≤ 10pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Mode	t_{ODLY}		14	ns	C_L ≤ 40pF (1 card)
Output	t_{OH}	2.5		ns	C_L ≥ 15pF (1 card)
Total each line	C_L		40	pF	1 card

Note1:

In order to satisfy sever timing , host shall drive only one card.

5.2 For 1.8V Signaling

5.2.1 Threshold Level for High Voltage Range

Table 8. Threshold Level for High Voltage

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4		V	I_{OH} = -2mA
Output Low Voltage	V_{OL}		0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.0	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.58	V	

5.2.2 Peak Voltage and Leakage Current

Table 9. Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected

5.2.3 Bus Timing Specification in SDR12, SDR25, SDR50 and SDR104 Modes

I Clock Timing

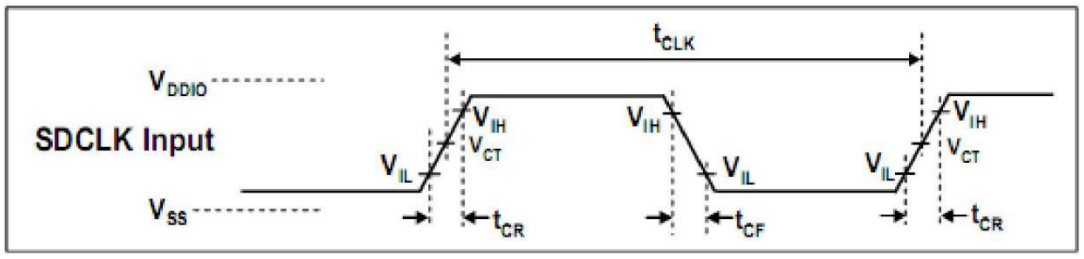

Figure 6. Clock Signal Timing

Table 10. Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, V_{CT}=0.975V
t_{CR}, t	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value oft_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

Card Input Timing

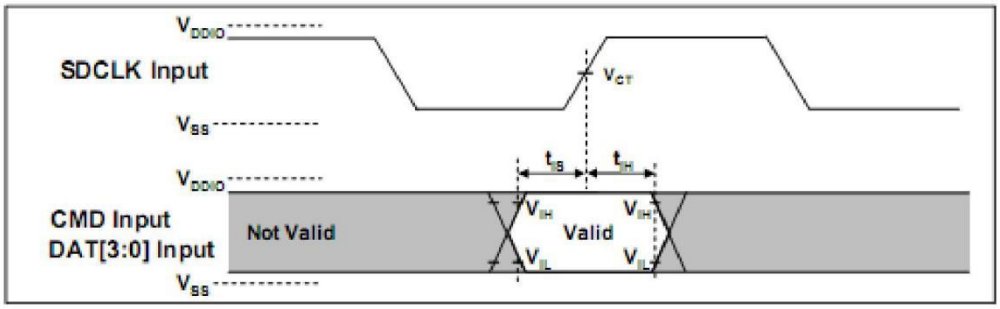

Figure 7. Card Input Timing

Table 11. SDR50 and SDR104 Input Timing

Symbol	Min	Max	Unit	SDR104 mode
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80		ns	C_{CARD} = 5pF, V_{CT} = 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR12, SDR25 and SDR50 modes**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)

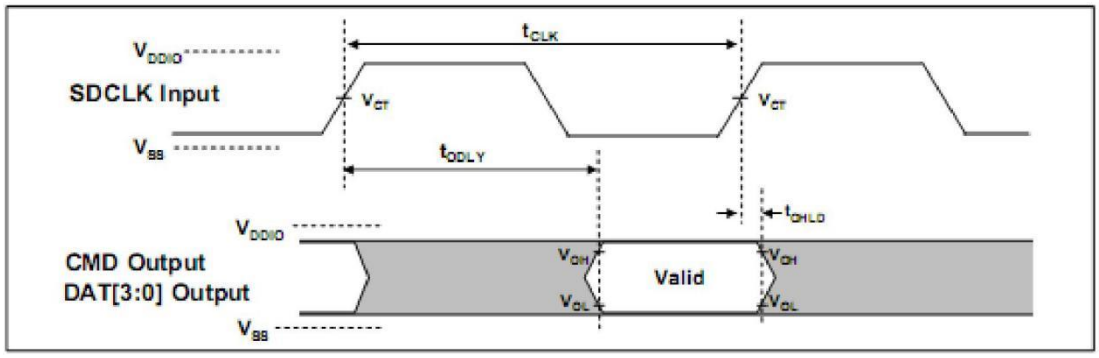

Figure 8. Output Timing of Fixed Data Window

Table 12. Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, C_L=30pF, using driver Type B, for SDR50.
t_{ODLY}		14	ns	t_{CLK} ≥20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12.
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). C_L=15pF

l Output Timing of Variable Window (SDR104)

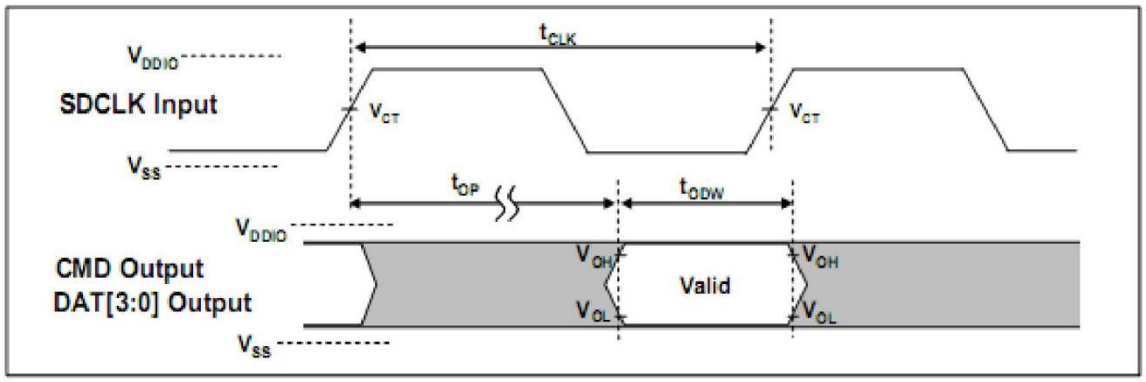

Figure 9. Output Timing of Variable Data Window

Table 13. Output Timing of Variable Data Window

Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

5.2.4 Bus Timing Specification in DDR50 Mode

l Clock Timing

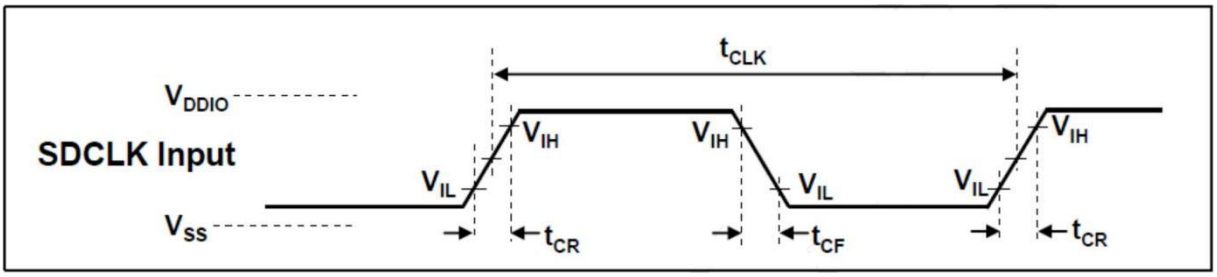

Figure 10. Clock Signal Timing

Table 14.Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} <4.00ns(max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	

Bus Timing for DDR50

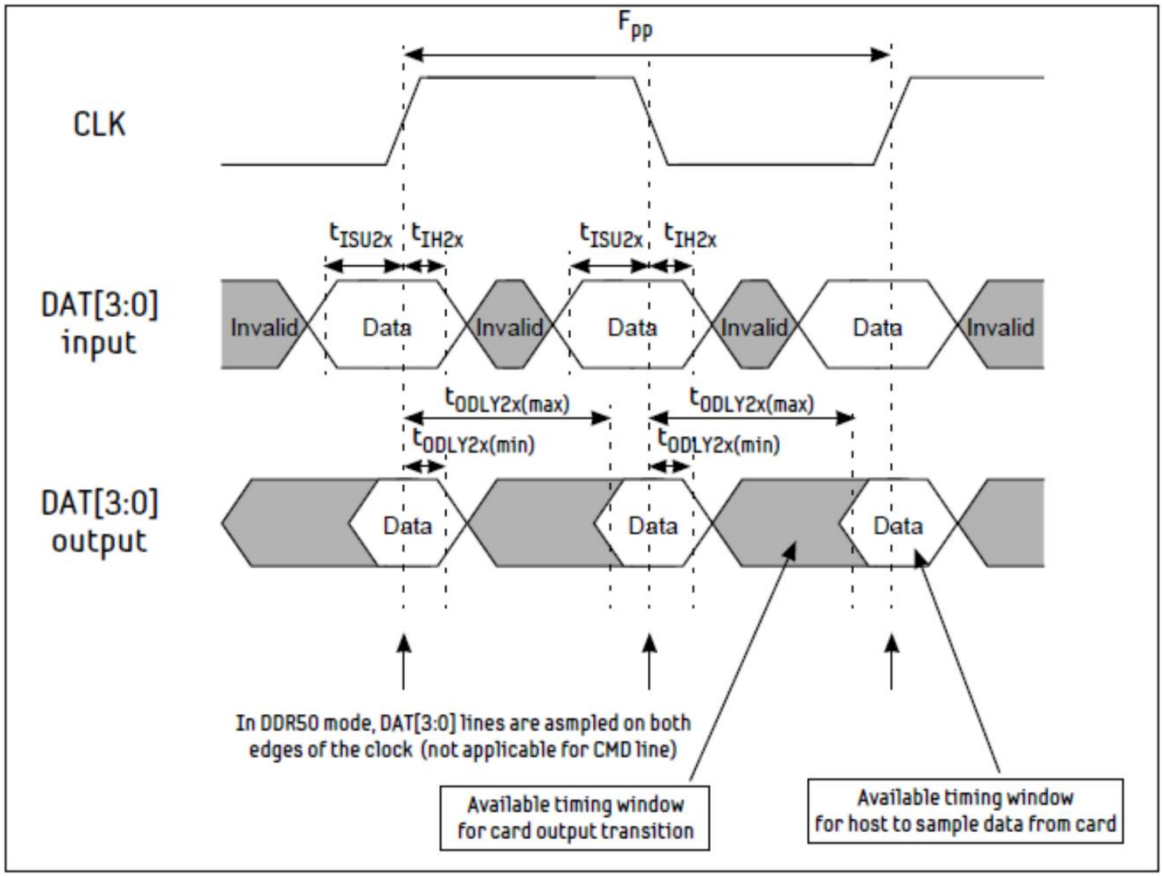

Figure 11. Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Table 15. Bus Timings - Parameters Values (DDR50 mode)

Parameter	Symbol	Min.	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_{CARD} ≤ 10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD} ≤ 10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	C_L ≤ 30pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	C_L ≥ 15pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{CARD} ≤ 10pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{CARD} ≤ 10pF (1 card)
Output CMD (referenced to CLK rising and failing edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L ≤ 25pF (1 card)
Output hold time	t_{ODLY2x}	1.5	-	ns	C_L ≥ 15pF (1 card)

6 Physical Dimension

Table 19. Physical Dimension Specifications (Unit in mm)

Type	Measurement
Length	15mm +/- 0.1mm(B)
Width	11mm +/- 0.1mm(A)
Thickness	1.0mm+/-0.1mm(C)
	0.7mm+/-0.1mm(C1)
Weight	0.33 gram Max

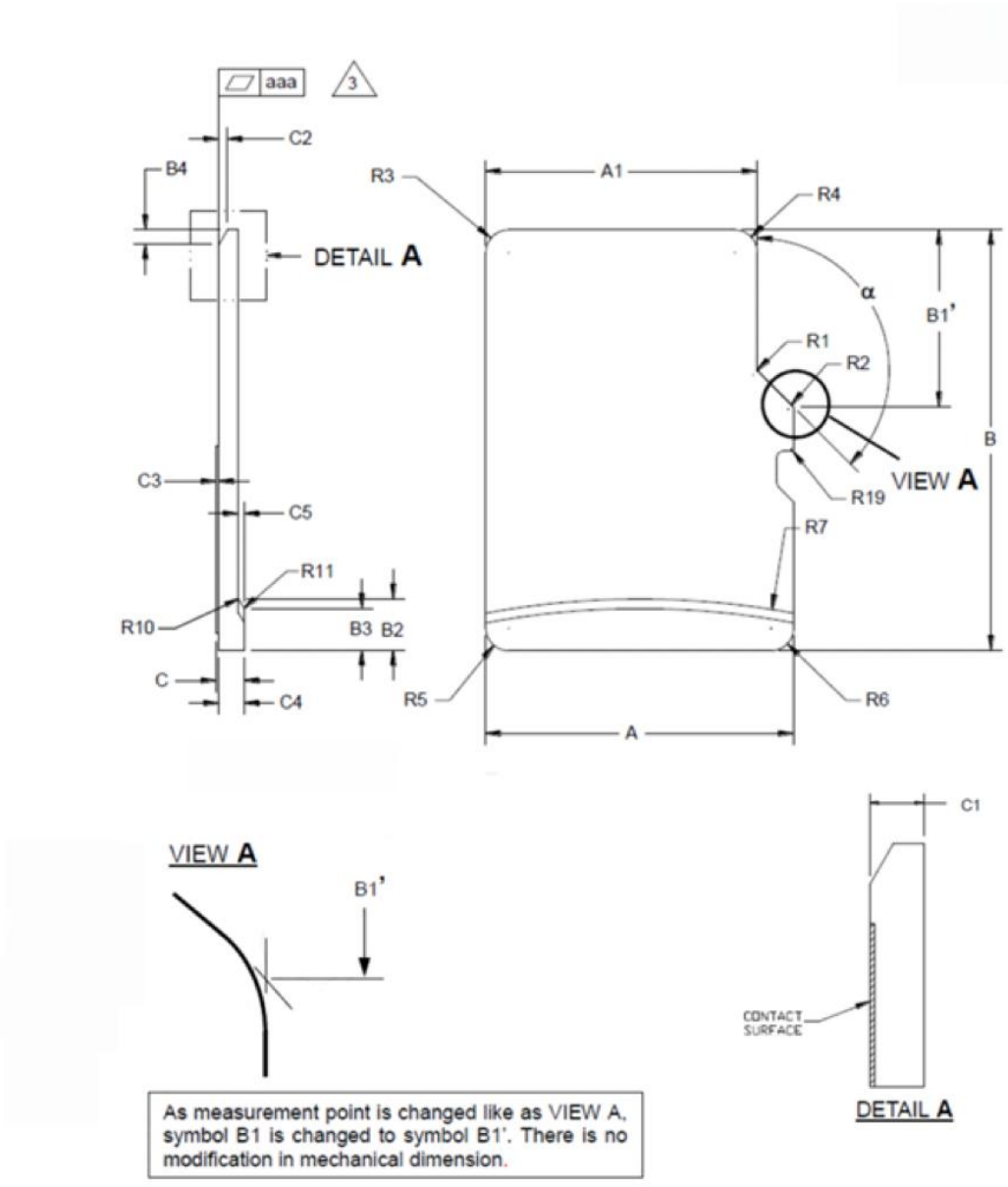

Figure 12. Mechanical Description: Top View

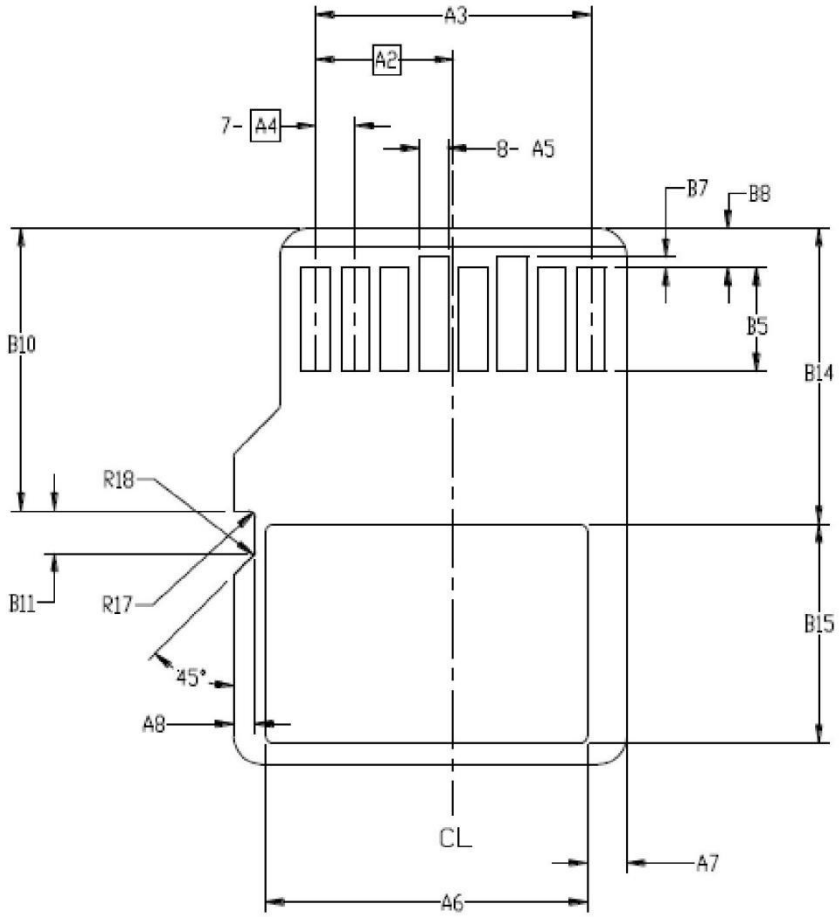

Figure 13. Mechanical Description: Bottom View

Table 20. microSD Package: Dimensions

SYMBOL	MIN (mm)	NOM (mm)	MAX (mm)	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
B	14.90	15.00	15.10	
B1,	6.13	6.23	6.33	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B7	0.20	0.30	0.40	

B8	1.00	1.10	1.20	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
C4	0.80	-	1.10	
C5	0.15	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	

