DDR5 UDIMM 16GB 1RX8 5600 Datasheet

TMD5UHAAD1656S-00N0

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Key Features

Standard Reference

- JEDEC Standard No. JESD79-5

Supported Features

- On-DIMM SPD EEPROM with hub function and integrated temperature sensor (TS)
- On-DIMM Power Management Integrated Circuit (PMIC)
- DRAM VDD/VDDQ = 1.1V (-33mV / + 66mV)
- DRAM VPP = 1.8V (-54mV / + 108mV)
- 16n-bit pre-fetch
- BL16, BC8 OTF, BL32, BL32 OTF supported
- VrefDQ / VrefCA / VrefCS Training
- CRC (Cyclic Redundancy Check)
- On-Die ECC
- Halogen-free
- Fly-by topology
- Golden Finger: 30μ''
- Raw card:A0
- Anti-Sulfuration
- Operating temperature: -40~85℃(-W), -25~85℃(-M), 0~85℃(-S)

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1. Introduction

1.1 General Description

The Unbuffered DDR5 SDRAM DIMM (Unbuffered Double Data Rate Syn-chronous DRAM Dual In-Line Memory Module) is a low power, high-speed operation memory module. The DDR5 SDRAM Unbuffered DIMM is designed to be installed in personal computers.

1.2 Product Line-up

Table 1 Product Line-up

Part Number	Density	Speed	Component Composition	# of Ranks
TMD5UHAAD1656S-00N0	16GB	DDR5-5600	2Gx8*8	1

1.3 Key Parameters

Table 2 Key Parameters

Grade	Speed (Mbps)	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
5600B	5600	0.357	46	16.000	16.000	32.000	48.000	46-45-45

Table 3 Address Table

Organization	Number of Bank Groups	Bank Group Address	Bank Address in Bank Group	Row Address	Column Address
2Gx8	8	BG0~BG2	BA0~BA1	R0~R15	C0~C9

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1.4 Part Number Decoder

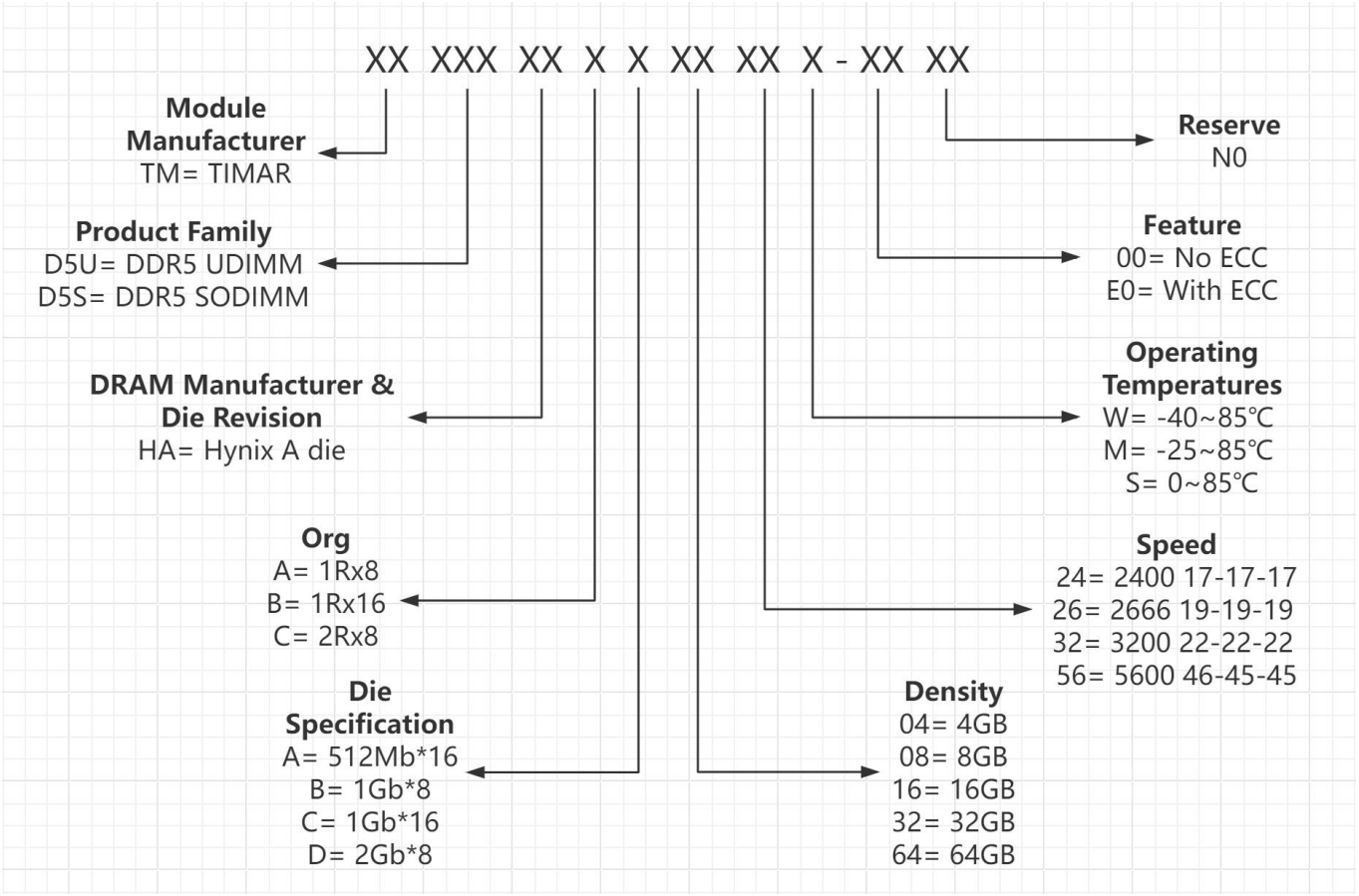

Figure 1 Part Number Decoder

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2. Product Specifications

2.1 Pin Description

Table 4 Pin Description

Pin Name	Description	Pin Name	Description
CA0_A - CA12_A	Command/Address input to channel A	CA0_B - CA12_B	Command address input to channel B
CS0_A_n, CS1_A_n	DIMM Rank Select Lines input for channel A	CS0_B_n, CS1_B_n	DIMM Rank Select Lines input for channel B
DQ0_A - DQ31_A	DIMM memory data bus for channel A.	DQ0_B - DQ31_B	DIMM memory data bus for channel B
CB0_A - CB3_A	DIMM ECC check bits for channel A. (For ECC UDIMM)	CB0_B - CB3_B	DIMM ECC check bits for channel B. (for ECC UDIMM)
CK0_A_t, CK1_A_t	SDRAM clock for channel A. (positive line of differential pair)	CK0_B_t, CK1_B_t	SDRAM clock for channel B. (positive line of differential pair)
CK0_A_c, CK1_A_c	SDRAM clock for channel A. (negative line of differential pair)	CK0_B_c, CK1_B_c	SDRAM clock for channel B. (negative line of differential pair)
DQS0_A_t - DQS4_A_t	Data Buffer data strobes in channel A.(positive line of differential pair)	DQS0_B_t - DQS4_B_t	Data Buffer data strobes in channel B.(positive line of differential pair)
DQS0_A_c - DQS4_A_c	Data Buffer data strobes in channel A.(negative line of differential pair)	DQS0_B_c - DQS4_B_c	Data Buffer data strobes in channel B.(negative line of differential pair)
DM0_A_n - DM3_A_n	SDRAM input data mask signal for write data of channel A.	DM0_B_n - DM3_B_n	SDRAM input data mask signal for write data of channel B.
VIN_BULK	5 V power input supply pin to the PMIC	VSS	Power supply return (ground)
PWR_GOOD	Output for Power good indicator from the PMIC. The PMIC ensures this pin high when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. Otherwise PMIC will drive this pin low. The PMIC disables its output regulator when this pin is low	PWR_EN	Power Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator.
HSCL	Side-band bus serial bus clock for SPD-Hub.	RESET_n	Set Register and SDRAMs to a Known State
HSDA	Side-band bus serial data line for SPD-Hub.	ALERT_n	Register ALERT_n output
HSA	Side-band bus Host ID and Hub device type ID selection.	RFU	Reserved for future use

2.2 Input/Output Function Description

Table 5 Input/Output Function Description

Symbol	Type	Function
CK0_A_t, CK0_A_c CK1_A_t,CK1_A_c, CK0_B_t, CK0_B_c CK1_B_t, CK1_B_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A, CA12_A CA0_B, CA12_B	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus.
CS0_A_n - CS1_A_n, CS0_B_n - CS1_B_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DQ0_A - DQ31_A, DQ0_B - DQ31_B	Input/Output	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB0_A - CB3_A, CB0_B - CB3_B	Input/Output	DIMM ECC check bits
DQS0_A_t,DQS4_A_t DQS0_A_c,DQS4_A_c DQS0_B_t,DQS4_B_t DQS0_B_c,DQS4_B_c	Input/Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n-DM3_A_n, DM0_B_n-DM3_B_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
ALERT_n	Input/Output	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
HSCL	Input	Host SidebandBus bus clock, supplied by the master.
HSDA	Input/Output	Host SidebandBus data, connected from the master to bubs or host bus client devices.
HSA	Input	Host SidebandBus bus device ID. Address input to a hub or other clientdevices to distinguish between identical devices in the I3C-Basic/I2C addressrange.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
PWR_EN	Input	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This pin shall not be left floating. If it is not used, it shall be tied to GND.
PWR_GOOD	Input/Output	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or configured in the appropriate register or and LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
VIN_BULK	Supply	5V power input supply to the PMIC for analog circuits.
VSS	Supply	Ground

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2.3 Pin Assignment

Table 6 Pin Assignment

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VIN_BULK	145	VIN_BULK	75	RFU	219	RFU
2	RFU	146	VIN_BULK	KEY			
3	RFU	147	PWR_GOOD	76	RFU	220	RFU
4	HSCL	148	HSA	77	VSS	221	VSS
5	HSDA	149	RFU	78	CK0_B_t	222	CK1_B_t
6	VSS	150	VSS	79	CK0_B_c	223	CK1_B_c
7	RFU	151	PWR_EN	80	VSS	224	VSS
8	VSS	152	RFU	81	RFU	225	RFU
9	DQ0_A	153	VSS	82	CA12_B	226	RFU
10	VSS	154	DQ2_A	83	VSS	227	VSS
11	DQ1_A	155	VSS	84	CA10_B	228	CA11_B
12	VSS	156	DQ3_A	85	CA8_B	229	CA9_B
13	DQS0_A_c	157	VSS	86	VSS	230	VSS
14	DQS0_A_t	158	DM0_A_n	87	CA6_B	231	CA7_B
15	VSS	159	VSS	88	CA4_B	232	CA5_B
16	DQ4_A	160	DQ6_A	89	VSS	233	VSS
17	VSS	161	VSS	90	CA2_B	234	CA3_B
18	DQ5_A	162	DQ7_A	91	CA0_B	235	CA1_B
19	VSS	163	VSS	92	VSS	236	VSS
20	DQ8_A	164	DQ10_A	93	CS0_B_n	237	CS1_B_n
21	VSS	165	VSS	94	VSS	238	VSS
22	DQ9_A	166	DQ11_A	95	RESET_n	239	DQS4_B_c
23	VSS	167	VSS	96	VSS	240	DQS4_B_t
24	DM1_A_n	168	DQS1_A_c	97	CB0_B	241	VSS
25	VSS	169	DQS1_A_t	98	VSS	242	CB2_B
26	DQ12_A	170	VSS	99	CB1_B	243	VSS
27	VSS	171	DQ14_A	100	VSS	244	CB3_B
28	DQ13_A	172	VSS	101	DQ0_B	245	VSS
29	VSS	173	DQ15_A	102	VSS	246	DQ2_B
30	DQ16_A	174	VSS	103	DQ1_B	247	VSS
31	VSS	175	DQ18_A	104	VSS	248	DQ3_B
32	DQ17_A	176	VSS	105	DQS0_B_c	249	VSS
33	VSS	177	DQ19_A	106	DQS0_B_t	250	DM0_B_n
34	DQS2_A_c	178	VSS	107	VSS	251	VSS
35	DQS2_A_t	179	DM2_A_n	108	DQ4_B	252	DQ6_B
36	VSS	180	VSS	109	VSS	253	VSS

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Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
37	DQ20_A	181	DQ22_A	110	DQ5_B	254	DQ7_B
38	VSS	182	VSS	111	VSS	255	VSS
39	DQ21_A	183	DQ23_A	112	DQ8_B	256	DQ10_B
40	VSS	184	VSS	113	VSS	257	VSS
41	DQ24_A	185	DQ26_A	114	DQ9_B	258	DQ11_B
42	VSS	186	VSS	115	VSS	259	VSS
43	DQ25_A	187	DQ27_A	116	DM1_B_n	260	DQS1_B_c
44	VSS	188	VSS	117	VSS	261	DQS1_B_t
45	DM3_A_n	189	DQS3_A_c	118	DQ12_B	262	VSS
46	VSS	190	DQS3_A_t	119	VSS	263	DQ14_B
47	DQ28_A	191	VSS	120	DQ13_B	264	VSS
48	VSS	192	DQ30_A	121	VSS	265	DQ15_B
49	DQ29_A	193	VSS	122	DQ16_B	266	VSS
50	VSS	194	DQ31_A	123	VSS	267	DQ18_B
51	CB0_A	195	VSS	124	DQ17_B	268	VSS
52	VSS	196	CB2_A	125	VSS	269	DQ19_B
53	CB1_A	197	VSS	126	DQS2_B_c	270	VSS
54	VSS	198	CB3_A	127	DQS2_B_t	271	DM2_B_n
55	DQS4_A_c	199	VSS	128	VSS	272	VSS
56	DQS4_A_t	200	ALERT_n	129	DQ20_B	273	DQ22_B
57	VSS	201	VSS	130	VSS	274	VSS
58	CS0_A_n	202	CS1_A_n	131	DQ21_B	275	DQ23_B
59	VSS	203	VSS	132	VSS	276	VSS
60	CA0_A	204	CA1_A	133	DQ24_B	277	DQ26_B
61	CA2_A	205	CA3_A	134	VSS	278	VSS
62	VSS	206	VSS	135	DQ25_B	279	DQ27_B
63	CA4_A	207	CA5_A	136	VSS	280	VSS
64	CA6_A	208	CA7_A	137	DM3_B_n	281	DQS3_B_c
65	VSS	209	VSS	138	VSS	282	DQS3_B_t
66	CA8_A	210	CA9_A	139	DQ28_B	283	VSS
67	CA10_A	211	CA11_A	140	VSS	284	DQ30_B
68	VSS	212	VSS	141	DQ29_B	285	VSS
69	CA12_A	213	RFU	142	VSS	286	DQ31_B
70	RFU	214	RFU	143	RFU	287	VSS
71	VSS	215	VSS	144	RFU	288	RFU
72	CK0_A_t	216	CK1_A_t				
73	CK0_A_c	217	CK1_A_c				
74	VSS	218	VSS				

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2.4 DQ Map

Table 7 DQ Map
*Description: DDRV SDRAM, Single-Rank, x8-FBGA 82-Ball-based, x64 Unbuffered, 288-pin UDIMM

Module Pin Number	Module DQ	IC No.	IC DQ	Module Pin Number	Module DQ	IC No.	IC DQ
9	0A	U00_A	1	20	8A	U01_A	1
11	1A		2	22	9A		2
154	2A		3	164	10A		3
156	3A		0	166	11A		0
16	4A		5	26	12A		5
18	5A		6	28	13A		6
160	6A		7	171	14A		7
162	7A		4	173	15A		4
30	16A	U02_A	1	41	24A	U03_A	1
32	17A		2	43	25A		2
175	18A		3	185	26A		3
177	19A		0	187	27A		0
37	20A		5	47	28A		5
39	21A		6	49	29A		6
181	22A		7	192	30A		7
183	23A		4	194	31A		4
101	0B	U00_B	1	112	8B	U01_B	1
103	1B		2	114	9B		2
246	2B		3	256	10B		3
248	3B		0	258	11B		0
108	4B		5	118	12B		5
110	5B		6	120	13B		6
252	6B		7	263	14B		7
254	7B		4	265	15B		4
122	16B	U02_B	1	133	24B	U03_B	1
124	17B		2	135	25B		2
267	18B		3	277	26B		3
269	19B		0	279	27B		0
129	20B		5	139	28B		5
131	21B		6	141	29B		6
273	22B		7	284	30B		7
275	23B		4	286	31B		4

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2.5 Speed Bins

Table 8 DDR5-5600 Speed Bin and Operations

DDR5-5600 Speed Bin							Unit
CL-nRCD-nRP					46-45-45		Unit
Parameter				Symbol	Min	Max	Unit
Internal READ command to first data				tAA	16.000	22.222	ns
ACTIVATE to internal READ or WRITE delay time				tRCD	16.000	–	ns
PRECHARGE command period				tRP	16.000	–	ns
ACTIVATE-to-PRECHARGE command period				tRAS	32.000	5 x tREFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period				tRC	48.000	–	ns
CAS Write Latency				CWL	CL-2		tCK
Speed Bin	**tAAmin**	**tRCD tRP**	**Read CL Write CWL**	**Supported Frequency Table**			
3200C	17.500	17.500	CL=28, CWL=26	tCK(AVG)	0.625	0.681	ns
3200BN 3200B	16.250	16.250	CL=26, CWL=24	tCK(AVG)	0.625	0.681	ns
3200AN	15.000	15.000	CL=24, CWL=22	tCK(AVG)	Reserved		ns
3600C	17.777	17.777	CL=32, CWL=30	tCK(AVG)	0.555	<0.625	ns
3600BN 3600B	16.666	16.666	CL=30, CWL=28	tCK(AVG)	0.555	<0.625	ns
3600AN	14.444	14.444	CL=26, CWL=24	tCK(AVG)	Reserved		ns
4000C	18.000	17.500	CL=36, CWL=34	tCK(AVG)	0.500	<0.555	ns
4000BN 4000B	16.000	16.000	CL=32, CWL=30	tCK(AVG)	0.500	<0.555	ns
4000AN	14.000	14.000	CL=28, CWL=26	tCK(AVG)	Reserved		ns
4400C	18.181	17.727	CL=40, CWL=38	tCK(AVG)	0.454	<0.500	ns
4400BN 4400B	16.363	16.363	CL=36, CWL=34	tCK(AVG)	0.454	<0.500	ns
4400AN	14.545	14.545	CL=32, CWL=30	tCK(AVG)	Reserved		ns
4800C	17.500	17.500	CL=42, CWL=40	tCK(AVG)	0.416	<0.454	ns
4800BN	16.666	16.666	CL=40, CWL=38	tCK(AVG)	0.416	<0.454	ns
4800B	16.666	16.250	CL=40, CWL=38	tCK(AVG)	0.416	<0.454	ns
4800AN	14.166	14.166	CL=34, CWL=32	tCK(AVG)	Reserved		ns
5200C	17.692	17.692	CL=46, CWL=44	tCK(AVG)	0.384	<0.416	ns
5200BN,B	16.153	16.153	CL=42, CWL=40	tCK(AVG)	0.384	<0.416	ns
5200AN	14.615	14.615	CL=38, CWL=36	tCK(AVG)	Reserved		ns
5600C	17.857	17.500	CL=50, CWL=48	tCK(AVG)	0.357	<0.384	ns
5600BN	16.428	16.428	CL=46, CWL=44	tCK(AVG)	0.357	<0.384	ns
5600B	16.428	16.071	CL=46, CWL=44	tCK(AVG)	0.357	<0.384	ns
5600AN	14.285	14.285	CL=40, CWL=38	tCK(AVG)	Reserved		ns
Supported CL Settings					22, 26, 28, 30, 32, 36, 40, 42, 46, 50		nCK

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2.6 DRAM Component Operating Temperature Range

Table 9 Temperature Range

Symbol	Parameter	Rating	Unit	Grade
T_{OPER}	DRAM Operating Temperature	0 to 85	℃	NT
$T_{EXTENDED}$	Extended Operating Temperature	0 to 95	℃	XT

Notes:
1.All operating temperature symbols, ranges, acronyms are referred from JESD402-1.
2.Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3.All DDR5 SDRDAMs are required to operate in NT and XT temperature ranges.
4.When operating above 85°C, the host shall provide appropriate Refresh mode controls associated with the increased temperature range. The full description of these settings are defined in JESD79-5B.

Table 10 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.4	V
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.4	V
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.1	V
VIN, VOUT	Voltage on any relative to VSS	-0.3 ~ 1.4	V
VSTG	Storage Temperature	-55 to +100	℃

Notes:
1.Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2.Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Table 11 DC Operating Conditions

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
VDD	Device Supply Voltage	1.067	1.1	1.166	V
VDDQ	Supply Voltage for I/O	1.067	1.1	1.166	V
VPP	Core Power Voltage	1.746	1.8	1.908	V

Note:
1.VDD must be within 66mv of VDDQ.

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2.7 Functional Diagram

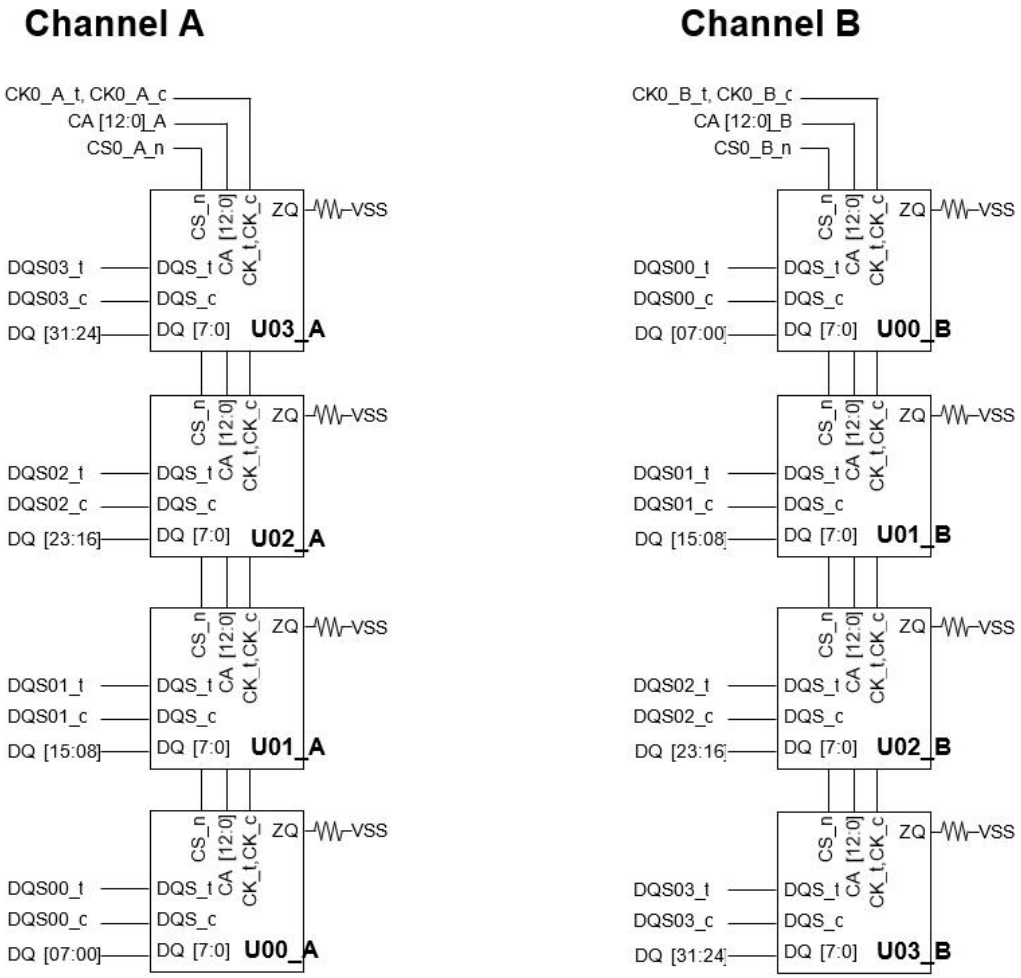
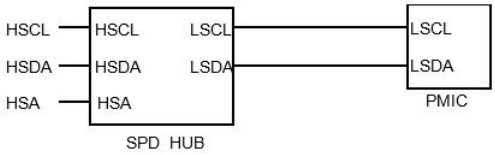


Figure 2 Functional Diagram (Ⅰ)



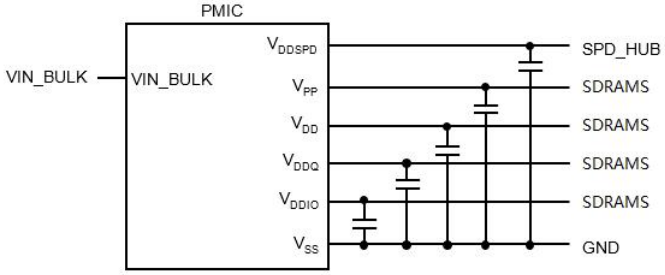


Figure 3 Functional Diagram (Ⅱ)

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3. PCB Specifications

3.1 General Specifications

1.Board size：133.35 x 31.25 mm

2.Thickness：1.27 ± 0.1 mm

3.Pin count：288 PIN

3.2 Module Dimension

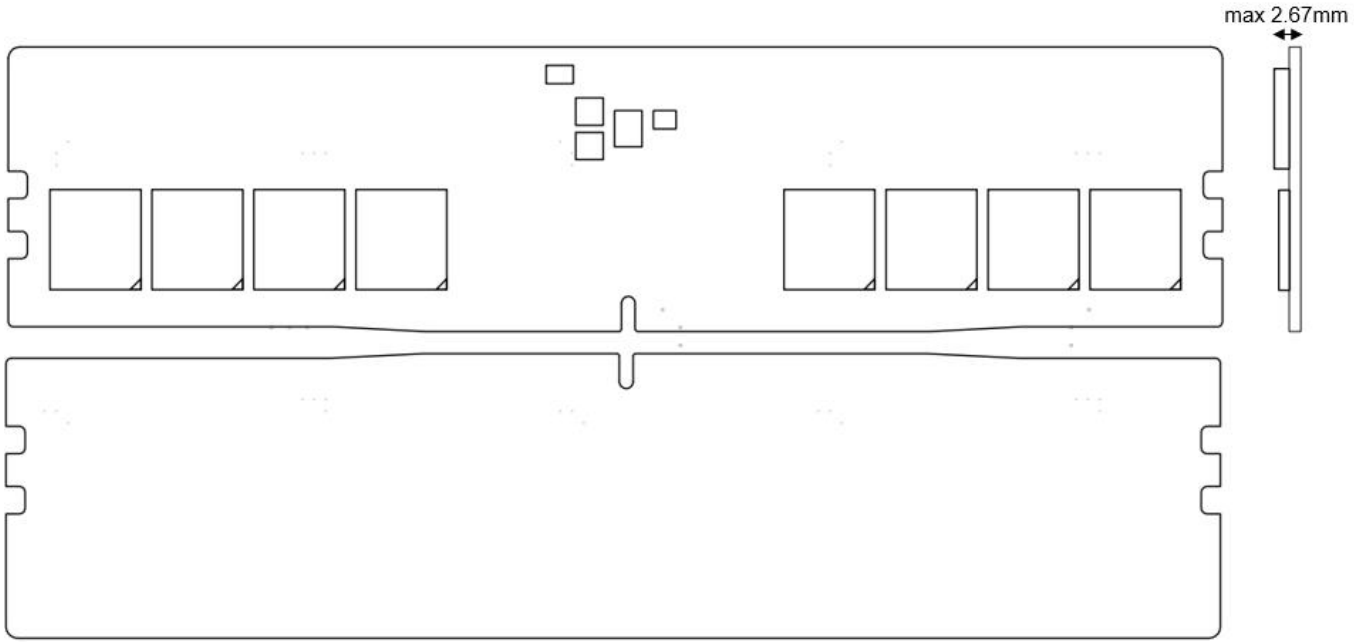

Figure 4 Module Dimension in Millimeters

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Revision History

Version	Date	Changes
1.0	2025.4	Initial Release

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